21.6 A 3.5GHz Rotary-Traveling-Wave-Oscillator Clocked Dynamic Logic Family in 0.25μm CMOS

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The first silicon measurements of a 3.5GHz fully pipelined dynamic logic family that utilizes only NMOS devices in a 0.25μm SOI process are presented. A key feature of the test-chip involves the use of the rotary traveling wave oscillator (RTWO) [1, 2, 3, 4] as clock and power source for the logic family. This oscillator topology has previously been demonstrated in a variety of processes and frequency ranges including a 36GHz low-phase-noise oscillator in 0.13μm CMOS [5]. Given the demonstrated scalability, low inherent jitter, and uncertainty of the RTWO as well as the 3.5GHz performance reported in this work from a 0.25μm SOI process, it is clear that there is a potential for significantly higher throughputs compared to other techniques when scaled to more modern processes.

Previous clock-powered logic families [6] focused on using a resonant or harmonically driven clock to provide ultra-low power consumption at the expense of performance. At much higher frequencies, however, similar techniques using the RTWO enable, the drastic reduction of clock uncertainty and clock dissipation, two factors that may limit conventional digital design techniques as frequencies exceeds multi-GHz. Combining the square wave, multi-GHz, multi-phase clocks from a RTWO with the special transistor characteristics of SOI technologies, has enabled the creation of an NMOS-only logic family, called clock-steered logic (CSL). A set of RTWO-powered CSL test structures, including a buffer/inverter gate, a 2-input AND/OR/NAND/NOR gate, and a 2-input XOR/XNOR gate, are recently designed, fabricated, and tested. The logic family is tested to be functionally correct across a frequency range from 2.8 to 3.5GHz with per-gate fanouts of 1 to 5.

The Clock-Steered logic family is a dual-rail two-clock-phase logic family. The logic family is designed to be driven by an RTWO (transmission-line oscillator), utilizing its properties of high drive capability, non-overlapping differential output, full swing, fast rise and fall times, and relative insensitivity to locally varying load conditions. The RTWO is capable of providing a differential clock distribution network to a system of arbitrary size. The RTWO is a simple circuit, and its design is easily transferred from bulk CMOS to SOI without modification, and with the benefit of having no appreciable loss mechanisms in the substrate. The CSL circuit is powered entirely by this oscillator, with no separate V_{dd} supply.

The choice of an SOI process allows use of NMOS transistors as pass-gates for gating the clock signal, allowing the entire circuit to be constructed from only NMOS transistors. There are also RTWO circuit designs that only use NMOS transistors, so potentially, an entire system may be realized in NMOS-only technology.

A typical series-parallel gate that can be used to implement any of the functions (AND,NAND,OR,NOR) is shown in Fig. 21.6.1. Each gate is composed of three parts: 1) a set of input switches, 2) the dual-rail evaluation tree, and 3) a cross-coupled output stage. The minimum-size input switches capture the complementary logic inputs (*at, af*) and (*bt, bf*) on the first clock phase, *clkt*, storing the captured charge on the gate capacitance of the evaluation-tree transistors. The evaluation tree, a standard series-parallel implementation of the logic function and its complement, is clocked on the second clock phase, *clkf*, passing the clock logic high value to the appropriate (complementary) output. A pair of cross-coupled nFETs on the output lines restores the logic low state, forcing the un-driven output to be pulled down to ground. While the pass gate connection to the clock implies a data-dependent clock-load, the dual-rail design balances this data-dependency and the RTWO is stable under small data-dependent capacitance mismatches.

A CSL logic pipeline is composed of an even number of gates whose clock inputs are alternated, as in a typical dynamic logic family such as domino CMOS, with outputs stable for one-half of a clock cycle. A pipeline of gates connected to the rotary clock is shown in Fig. 21.6.2. Typical (simulated) output waveforms of the series-parallel gate are shown in Fig. 21.6.3.

A small test chip is designed in a 3M 0.25μm SOI process. The test chip consists of a RTWO and 8 CSL test structures distributed around the clock wires, as shown in Fig. 21.6.4. Each CSL test structure consists of a pattern generator, a gate under test with specific fanout, and a CSL buffer chain amplifying the output signal to drive a 50Ω probe pad. The 2-input AND/OR and the XOR gates as well as the single-input BUF gate for fanouts between 3 to 5 are tested. Each gate is verified for correct operation using a sampling oscilloscope, as shown in Fig. 21.6.5.

Differential power measurements are obtained by measuring the total system power before and after blowing laser-fuses connecting each CSL test structure to the clock. These power measurements represent the entire power dissipated in the CSL test structure, including the power used to drive the 50Ω passive probe. These measured power dissipations are in agreement with that of the simulated CSL test structures within 20% of simulated results for the same test structure. The power delivered to the 50Ω probe dominates the CSL test structure power. Therefore, the measurement precision of power dissipation for individual gates is limited and accurate per-gate power dissipation measurements could not be obtained. As a result, only simulated per-gate dissipations are provided in Fig. 21.6.6.

References:

[1] J. Wood, T. Edwards, S. Lipa, "Rotary Traveling-Wave Oscillator Arrays: a New Clock Technology," *IEEE J. of Solid-State Circuits*, vol 36, no 11, pp. 1654-1665, Nov., 2001.

[2] J. Wood, "Electronic Circuitry," US Patent 6525618, Feb., 25, 2003.

[3] J. Wood, "Electronic Circuitry," US Patent 6556089, Apr., 29, 2003.

[4] J. Wood, "Electronics Circuits," WO 03/069452 (PCT/GB03/000719), Aug., 21, 2003

[5] G. Le Grand de Mercey, *"18GHz-36GHz Rotary Traveling Wave Voltage Controlled Oscillator in a CMOS Technology,"* PhD Thesis, Bundeswehr Universitat, Aug., 2004.

[6] W. C. Athas, et al., "A Low-Power Microprocessor Based on Resonant Energy," *IEEE J. of Solid-State Circuits*, vol. 32, no. 11, pp. 1693-1701, Nov., 1997.

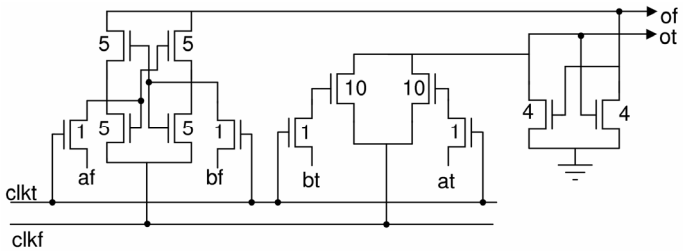

Figure 21.6.1: Schematic of series-parallel gate (AND/OR) with relative device sizes indicated.

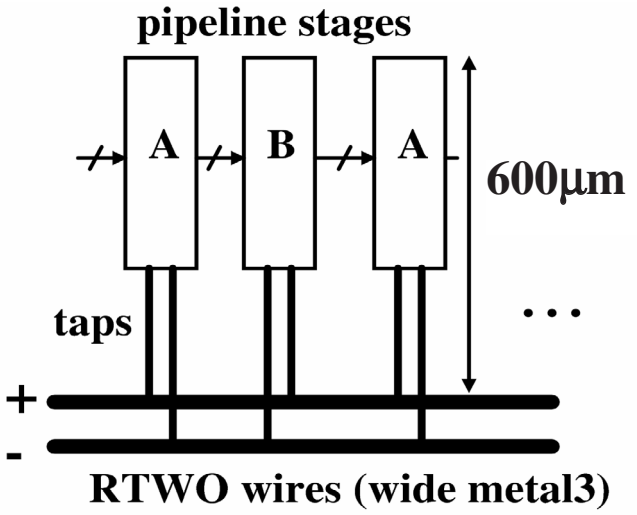

Figure 21.6.2: Pipeline and rotary clock wire interconnect detail.

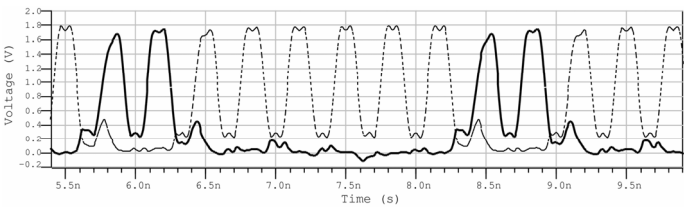

Figure 21.6.3: Simulated waveforms for typical gate.

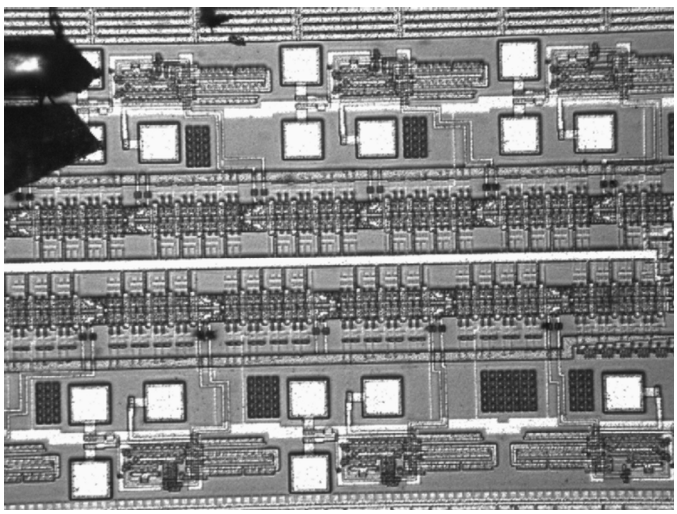

Figure 21.6.4: Die micrograph of test-chip showing RTWO oscillator with logic family test structures.

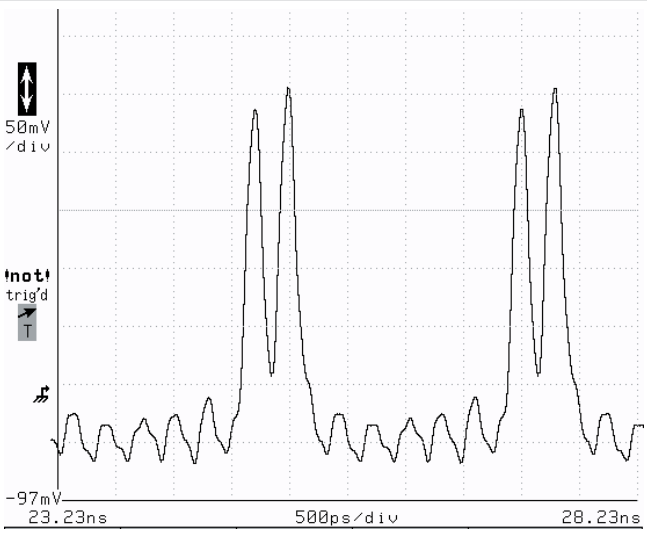

Figure 21.6.5: Measured voltage waveforms for period-8 self-test pattern at 3.5GHz from probed output of gate.

Voltage	Fanout	BUF	AND/OR	XOR
2.0V	3	65fJ	94fJ	169fJ
2.0V	4	80fJ	94fJ	210fJ
2.0V	5	98fJ	129fJ	255fJ
2.5V	3	129fJ	175fJ	315fJ
2.5V	4	154fJ	202fJ	444fJ
2.5V	5	183fJ	232fJ	521fJ

Figure 21.6.6: Simulated energy/operation at 3.5GHz in 0.25µm SOI process at indicated voltage and fanout ratios.